IEEE Xplore
RELEASE 2.1

Welcome United States Patent and Trademark Office

:□:**Search Results**

BROWSE   SEARCH   **IEEE XPLORE GUIDE**   SUPPOR°

Results for **"((processor and (programm* or configur* or reconfig* or architecture or creat* or build* or generat*..."**
Your search matched **20** of **1387402** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

☑ e-mail 🖶 printer i

» Search Options

View Session History
New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

[((processor and (programm* or configur* or reconfig* or architecture or creat* or bu|] Sea

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

[view selected items]   **Select All Deselect All**

☐ 1. **Selective victim caching: a method to improve the performanc direct-mapped caches**
Stiliadis, D.; Varma, A.;
System Sciences, 1994. Vol. I: Architecture, Proceedings of the Twenty-Seventh Hawaii Internation Conference on
Volume 1, 4-7 Jan. 1994 Page(s):412 - 421
Digital Object Identifier 10.1109/HICSS.1994.323144
AbstractPlus | Full Text: PDF(844 KB)   **IEEE CNF**
Rights and Permissions

☐ 2. **Higher performance and lower power enhancements to VLIW architectures**
Gass, W.;
Signal Processing Systems, 2001 IEEE Workshop on
26-28 Sept. 2001 Page(s):157
Digital Object Identifier 10.1109/SIPS.2001.957342
AbstractPlus | Full Text: PDF(45 KB)   **IEEE CNF**
Rights and Permissions

☐ 3. **Using virtual load/store queues (VLSQs) to reduce the negativ effects of reordered memory instructions**
Jaleel, J.; Jacob, B.;
High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on
12-16 Feb. 2005 Page(s):191 - 200
Digital Object Identifier 10.1109/HPCA.2005.42
AbstractPlus | Full Text: PDF(200 KB)   **IEEE CNF**
Rights and Permissions

☐ 4. **Balanced Cache: Reducing Conflict Misses of Direct-Mapped Caches**
Chuanjun Zhang;
Computer Architecture, 2006. 33rd International Symposium on

17-21 June 2006 Page(s):155 - 166
Digital Object Identifier 10.1109/ISCA.2006.12
AbstractPlus | Full Text: PDF(392 KB)   **IEEE CNF**
Rights and Permissions

☐ **5. Multilevel optimization of pipelined caches**
Olukotun, K.; Mudge, T.N.; Brown, R.B.;
Computers, IEEE Transactions on
Volume 46, Issue 10, Oct. 1997 Page(s):1093 - 1102
Digital Object Identifier 10.1109/12.628394
AbstractPlus | References | Full Text: PDF(424 KB)   **IEEE JNL**
Rights and Permissions

☐ **6. Branch prediction, instruction-window size, and cache size: performance trade-offs and simulation techniques**
Skadron, K.; Ahuja, P.S.; Martonosi, M.; Clark, D.W.;
Computers, IEEE Transactions on
Volume 48, Issue 11, Nov. 1999 Page(s):1260 - 1281
Digital Object Identifier 10.1109/12.811115
AbstractPlus | References | Full Text: PDF(1880 KB)   **IEEE JNL**
Rights and Permissions

☐ **7. Trace cache sampling filter**
Behar, M.; Mendelson, A.; Kolodny, A.;
Parallel Architectures and Compilation Techniques, 2005. PACT 2(
14th International Conference on
17-21 Sept. 2005 Page(s):255 - 264
Digital Object Identifier 10.1109/PACT.2005.38
AbstractPlus | Full Text: PDF(176 KB)   **IEEE CNF**
Rights and Permissions

☐ **8. A multi-level block priority based instruction caching scheme multimedia processors**
Jiyang Kang; Wonyong Sung;
Signal Processing Systems, 2001 IEEE Workshop on
26-28 Sept. 2001 Page(s):125 - 132
Digital Object Identifier 10.1109/SIPS.2001.957338
AbstractPlus | Full Text: PDF(320 KB)   **IEEE CNF**
Rights and Permissions

☐ **9. Cache memories for data flow machines**
Takesue, M.;
Computers, IEEE Transactions on
Volume 41, Issue 6, June 1992 Page(s):677 - 687
Digital Object Identifier 10.1109/12.144620
AbstractPlus | Full Text: PDF(952 KB)   **IEEE JNL**
Rights and Permissions

☐ **10. Memory hierarchy reconfiguration for energy and performanc general-purpose processor architectures**
Balasubramonian, R.; Albones, D.; Buyuktosunoglu, A.; Dwarkada S.;
Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual
IEEE/ACM International Symposium on
10-13 Dec. 2000 Page(s):245 - 257
Digital Object Identifier 10.1109/MICRO.2000.898075
AbstractPlus | Full Text: PDF(1128 KB)   **IEEE CNF**
Rights and Permissions

☐ **11. REMcode: relocating embedded code for improving system efficiency**
Janapsatya, A.; Parameswaran, S.; Henkel, J.;
Computers and Digital Techniques, IEE Proceedings-
Volume 151, Issue 6, 18 Nov. 2004 Page(s):457 - 465
Digital Object Identifier 10.1049/ip-cdt:20040942
AbstractPlus | Full Text: PDF(552 KB)   **IEE JNL**

☐ **12. Defying hard times [semiconductor intellectual property business]**
Dettmer, R.;
IEE Review
Volume 49, Issue 3, March 2003 Page(s):32 - 34
AbstractPlus | Full Text: PDF(432 KB)   **IEE JNL**

☐ **13. Analysis of control flow patterns in the execution of SPEC CPU2000 benchmark programs**
Joseph, P.J.; Matthew Jacob, T.;
TENCON 2003. Conference on Convergent Technologies for Asia Pacific Region
Volume 3, 15-17 Oct. 2003 Page(s):1143 - 1147 Vol.3
Digital Object Identifier 10.1109/TENCON.2003.1273426
AbstractPlus | Full Text: PDF(398 KB)   **IEEE CNF**
Rights and Permissions

☐ **14. A block priority based instruction caching scheme for multim processors**
Jiyang Kang; Wonyong Sung;
Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEEE International Conference on
Volume 2, 7-11 May 2001 Page(s):1117 - 1120 vol.2
Digital Object Identifier 10.1109/ICASSP.2001.941117
AbstractPlus | Full Text: PDF(320 KB)   **IEEE CNF**
Rights and Permissions

☐ **15. Hardware/software managed scratchpad memory for embedd system**
Andhi Janapsatya; Sri Parameswaran; Ignjatovic, A.;
Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM Internatic Conference on
7-11 Nov. 2004 Page(s):370 - 377
AbstractPlus | Full Text: PDF(923 KB)   **IEEE CNF**
Rights and Permissions

☐ **16. Efficient microarchitecture modeling and path analysis for re: time software**
Li, Y.-T.S.; Malik, S.; Wolfe, A.;
Real-Time Systems Symposium, 1995. Proceedings., 16th IEEE
5-7 Dec. 1995 Page(s):298 - 307
Digital Object Identifier 10.1109/REAL.1995.495219
AbstractPlus | Full Text: PDF(904 KB)   **IEEE CNF**
Rights and Permissions

☑ **17. Power efficient mediaprocessors: design space exploration**
Kin, J.; Chunho Lee; Mangione-Smith, W.H.; Potkonjak, M.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):321 - 326
Digital Object Identifier 10.1109/DAC.1999.781334

AbstractPlus | Full Text: PDF(596 KB)   **IEEE CNF**

Rights and Permissions

☐ **18. Power optimization of variable-voltage core-based systems**
Hong, I.; Kirovski, D.; Gang Qu; Potkonjak, M.; Srivastava, M.B.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE
Transactions on
Volume 18, Issue 12, Dec. 1999 Page(s):1702 - 1714
Digital Object Identifier 10.1109/43.811318
AbstractPlus | References | Full Text: PDF(288 KB)   **IEEE JNL**
Rights and Permissions

☐ **19. Optimal allocation of on-chip memory for multiple-API operat systems**
Nagle, D.; Uhlig, R.; Mudge, T.; Sechrest, S.;
Computer Architecture, 1994. Proceedings the 21st Annual
International Symposium on
18-21 April 1994 Page(s):358 - 369
Digital Object Identifier 10.1109/ISCA.1994.288135
AbstractPlus | Full Text: PDF(1000 KB)   **IEEE CNF**
Rights and Permissions

☐ **20. Power optimization of variable voltage core-based systems**
Inki Hong; Kirovski, D.; Gang Qu; Potkonjak, M.; Srivastava, M.B.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):176 - 181
AbstractPlus | Full Text: PDF(768 KB)   **IEEE CNF**
Rights and Permissions

Help   Contact Us   Priva
Security   IEEE

Indexed by
⚞ Inspec°